WHAT IS CLAIMED IS:

1. A sequential circuit comprising:

a plurality of memory elements, each of which updates its content in synchronization with a supplied clock, the plurality of memory elements including a memory element which functions as a master cell and a memory element which functions as a slave cell, an input to the slave cell being varied when a content of the master cell is varied;

variation detection means which outputs a variation signal when the content of the master cell is varied; and

a clock pulse generator for generating a clock pulse based on the variation signal and supplying the clock pulse to the slave cell as the supplied clock.

2. The sequential circuit of claim 1, further comprising:

a master cell group including at least one said master cell; and

a clock domain including at least one said slave cell whose input is varied when a content of any of the master cells included in the master cell group is varied,

wherein the variation detection means outputs the variation signal when a content of any of the master cells included in the master cell group is varied; and

the clock pulse generator supplies the clock pulse to all of the slave cells included in the clock domain.

3. The sequential circuit of claim 1, wherein the variation detection means is a variation detector which determines whether or not the content of the master cell is varied based on an output signal of the master cell and which outputs the variation signal when the

variation is detected.

4. The sequential circuit of claim 1, wherein:

the master cell is a memory element having a variation output, the memory element including a variation detection circuit which outputs an original variation signal indicative of a variation occurred in the content of the master cell; and

the variation detection means includes the variation detection circuit and outputs the variation signal based on the original variation signal output by the variation detection circuit.

5. The sequential circuit of claim 1, wherein:

the variation detection means includes a clock pulse generation request signal line for transmitting a request signal which requests the clock pulse generator to generate the clock pulse, the clock pulse generation request signal line changing the request signal to a first logic value when receiving the variation signal output by the variation detection means and changing the request signal to a second logic value when receiving a request update signal; and

the clock pulse generator is a clock pulse generator having an update output which generates the clock pulse and the request update signal when the request signal is changed to the first logic value, the request update signal being supplied to the clock pulse generation request signal line.

6. A memory element which updates its content in synchronization with a supplied clock, comprising:

a latch circuit which acquires a supplied signal when the supplied clock is

changed to a first logic value and which retains the acquired signal as the content of the memory element when the supplied clock is changed to a second logic value; and

a variation detection circuit which outputs a variation signal indicative of a variation occurred in the content of the memory element when the input and output of the latch circuit are different and the supplied clock is changed to the first logic value.

7. The memory element of claim 6, further comprising a master latch circuit which acquires a supplied signal when the supplied clock is changed to the second logic value and which retains the acquired signal when the supplied clock is changed to the first logic value, wherein:

the latch circuit is a slave latch circuit for acquiring a signal output from the master latch; and

the variation detection circuit includes

a first logic element which outputs a predetermined logic value when the input and output of the slave latch circuit are different

a delay element for delaying an output of the first logic element, and

a second logic element which outputs the variation signal when the output of the delay element is the predetermined logic value and the supplied clock has the first logic value.

8. The memory element of claim 6, wherein:

the variation detection circuit includes

a basic clock generation circuit for generating a basic clock which has a pulse width shorter than that of the supplied clock based on the supplied clock,

a first logic element which outputs a predetermined logic value when the input and output of the latch circuit are different, and

a second logic element which outputs the variation signal when an output of the first logic element is the predetermined logic value and the basic clock has the first logic value; and

the latch circuit receives the variation signal as the supplied clock.

9. A clock generation circuit for generating a clock pulse based on a request signal that requests generation of the clock pulse, comprising:

a clock pulse generator for generating the clock pulse; and

a clock pulse generation request signal line for transmitting the request signal to the clock pulse generator, which changes the request signal to a first logic value when receiving the request signal and which changes the request signal to a second logic value when receiving a request update signal,

wherein, when the request signal is changed to the first logic value, the clock pulse generator generates the clock pulse and generates the request update signal which is supplied to the clock pulse generation request signal line.

10. The clock generation circuit of claim 9,

the clock pulse generator receives an original clock which is the origin of the clock pulse; and

the clock pulse generator includes

a latch circuit which retains a predetermined logic value in synchronization with the falling of the original clock when the request signal is changed to the first logic value,

a first logic element which outputs a positive polarity pulse included in the original clock as the clock pulse when the logic value retained by the latch circuit is the predetermined logic value, and

a second logic element which outputs the request update signal in synchronization with the falling of the original clock when the request signal is changed to the first logic value.

11. The clock generation circuit of claim 9, wherein

the clock pulse generator receives an original clock which is the origin of the clock pulse; and

the clock pulse generator includes

a latch circuit which retains a predetermined logic value in synchronization with the rising of the original clock when the request signal is changed to the first logic value,

a first logic element which outputs a negative polarity pulse included in the original clock as the clock pulse when the logic value retained by the latch circuit is the predetermined logic value, and

a second logic element which outputs the request update signal in synchronization with the rising of the original clock when the request signal is changed to the first logic value.

12. A clock control method of a sequential circuit including a plurality of memory elements, each of which updates its content in synchronization with a supplied clock, comprising the steps of:

detecting a variation occurred in a content of a memory element included in

the plurality of memory elements; and

generating a clock pulse when the variation is detected and supplying the clock pulse as the supplied clock to any of the plurality of memory elements whose input is varied when the content of said memory element is varied.

13. A circuit modifying method for obtaining connection information of a new sequential circuit based on connection information of an original sequential circuit including a plurality of memory elements, each of which updates its content in synchronization with a supplied clock, the plurality of memory elements including a memory element which functions as a master cell and a memory element which functions as a slave cell, an input to the slave cell being varied when a content of the master cell is varied, the method comprising:

a slave cell extraction step of extracting the slave cell from connection information of the original sequential circuit;

a master cell group extraction step of extracting, for each extracted slave cell, a master cell group which includes at least one master cell corresponding to the slave cell from the connection information of the original sequential circuit;

a variation detection means generation step of generating connection information of variation detection means which outputs a variation signal when a content of any of the master cells included in the extracted master cell group is varied;

a clock pulse generator generation step of determining a clock domain so as to include some of the extracted slave cells whose extracted master cell groups are common, extracting a clock which is to be input to the slave cells included in the clock domain from connection information of the original sequential circuit, and generating connection information of a clock pulse generator based on the extracted clock; and

a connection information synthesizing step of synthesizing the connection information of the original sequential circuit, the connection information of the variation detection means which is generated at the variation detection means generation step, and the connection information of the clock pulse generator which is generated at the clock pulse generator generation step to obtain connection information of the new sequential circuit,

wherein the clock pulse generator generates a clock pulse as the clock extracted at the clock pulse generator generation step based on a variation signal output from the variation detection means.

14. The circuit modifying method of claim 13, wherein:

the variation detection means is a variation detector which determines whether or not the content of the master cell is varied based on an output signal of the master cell and which outputs the variation signal when the variation is detected; and

at the variation detection means generation step, one or more output signals of the at least one master cell included in the master cell group are extracted from the connection information of the original sequential circuit for each master cell group extracted at the master cell group extraction step, and connection information of the variation detector is generated based on the one or more extracted output signals.

15. The circuit modifying method of claim 13, wherein:

the master cell in the new sequential circuit is a memory element having a variation output, the memory element including a variation detection circuit which outputs an original variation signal indicative of a variation occurred in the content of the master cell;

the variation detection means includes the variation detection circuit and outputs the variation signal based on the original variation signal output by the variation detection circuit; and

at the variation detection means generation step, conversion information which is used for converting the at least one master cell included in the master cell group extracted at the master cell group extraction step to the memory element having a variation output is generated as the connection information of the variation detection means.

16. The circuit modifying method of claim 13, wherein:

the variation detection means includes a clock pulse generation request signal line for transmitting a request signal which requests the clock pulse generator to generate the clock pulse, the clock pulse generation request signal line changing the request signal to a first logic value when receiving the variation signal output by the variation detection means and changing the request signal to a second logic value when receiving a request update signal;

the clock pulse generator is a clock pulse generator having an update output which generates the clock pulse and the request update signal when the request signal is changed to the first logic value, the request update signal being supplied to the clock pulse generation request signal line;

the circuit modifying method comprises a clock pulse generator conversion step of generating conversion information used for converting the connection information of the clock pulse generator which is generated at the clock pulse generator generation step to connection information of the clock pulse generator having an update output; and

at the connection information synthesizing step, the connection information of the original sequential circuit, the connection information of the variation detection

means which is generated at the variation detection means generation step, the connection information of the clock pulse generator which is generated at the clock pulse generator generation step, and the conversion information generated at the clock pulse generator conversion step are synthesized to obtain connection information of the new sequential circuit.

17. A circuit-designing support system for obtaining connection information of a new sequential circuit based on connection information of an original sequential circuit including a plurality of memory elements, each of which updates its content in synchronization with a supplied clock, the plurality of memory elements including a memory element which functions as a master cell and a memory element which functions as a slave cell, an input to the slave cell being varied when a content of the master cell is varied, the system comprising:

slave cell extraction means for extracting the slave cell from connection information of the original sequential circuit;

master cell group extraction means for extracting, for each extracted slave cell, a master cell group which includes at least one master cell corresponding to the slave cell from the connection information of the original sequential circuit;

variation detection means-generation means for generating connection information of variation detection means which outputs a variation signal when a content of any of the master cells included in the extracted master cell group is varied;

clock pulse generator generation means for determining a clock domain so as to include some of the extracted slave cells whose extracted master cell groups are common, extracting a clock which is to be input to the slave cells included in the clock domain from connection information of the original sequential circuit, and generating

connection information of a clock pulse generator based on the extracted clock; and

connection information synthesizing means for synthesizing the connection information of the original sequential circuit, the connection information of the variation detection means which is generated by the variation detection means-generation means, and the connection information of the clock pulse generator which is generated by the clock pulse generator generation means to obtain connection information of the new sequential circuit,

wherein the clock pulse generator generates a clock pulse as the clock extracted by the clock pulse generator generation means based on a variation signal output from the variation detection means.

18. The circuit-designing support system of claim 17, wherein:

the variation detection means is a variation detector which determines whether or not the content of the master cell is varied based on an output signal of the master cell and which outputs the variation signal when the variation is detected; and

the variation detection means-generation means extracts one or more output signals of the at least one master cell included in the master cell group from the connection information of the original sequential circuit for each master cell group extracted by the master cell group extraction means to generate connection information of the variation detector based on the one or more extracted output signal.

19. The circuit-designing support system of claim 17, wherein:

the master cell in the new sequential circuit is a memory element having a variation output, the memory element including a variation detection circuit which outputs an original variation signal indicative of a variation occurred in the content of the master

cell;

the variation detection means includes the variation detection circuit and outputs the variation signal based on the original variation signal output by the variation detection circuit; and

the variation detection means-generation means generates conversion information which is used for converting the at least one master cell included in the master cell group extracted by the master cell group extraction means to the memory element having a variation output as the connection information of the variation detection means.

20. The circuit-designing support system of claim 17, wherein:

the variation detection means includes a clock pulse generation request signal line for transmitting a request signal which requests the clock pulse generator to generate the clock pulse, the clock pulse generation request signal line changing the request signal to a first logic value when receiving the variation signal output by the variation detection means and changing the request signal to a second logic value when receiving a request update signal;

the clock pulse generator is a clock pulse generator having an update output which generates the clock pulse and the request update signal when the request signal is changed to the first logic value, the request update signal being supplied to the clock pulse generation request signal line;

the circuit-designing support system comprises clock pulse generator conversion means for generating conversion information used for converting the connection information of the clock pulse generator which is generated by the clock pulse generator generation means to connection information of the clock pulse generator having an update output; and

the connection information synthesizing means synthesizes the connection information of the original sequential circuit, the connection information of the variation detection means which is generated by the variation detection means-generation means, the connection information of the clock pulse generator which is generated by the clock pulse generator generation means, and the conversion information generated by the clock pulse generator conversion means to obtain connection information of the new sequential circuit.

21. A semiconductor integrated circuit comprising a sequential circuit which includes a plurality of memory elements, each memory element updating its content in synchronization with a supplied clock, the plurality of memory elements including a memory element which functions as a master cell and a memory element which functions as a slave cell, an input to the slave cell being varied when a content of the master cell is varied,

wherein the sequential circuit includes:

variation detection means which outputs a variation signal when the content of the master cell is varied; and

a clock pulse generator for generating a clock pulse based on the variation signal and supplying the clock pulse to the slave cell as the supplied clock.

22. The semiconductor integrated circuit of claim 21, wherein the sequential circuit includes:

a master cell group including at least one said master cell; and

a clock domain including at least one said slave cell whose input is varied when a content of any of the master cells included in the master cell group is varied,

wherein the variation detection means outputs the variation signal when a

content of any of the master cells included in the master cell group is varied, and

the clock pulse generator supplies the clock pulse to all of the slave cells included in the clock domain.

23. The semiconductor integrated circuit of claim 21, wherein the variation detection means is a variation detector which determines whether or not the content of the master cell is varied based on an output signal of the master cell and which outputs the variation signal when the variation is detected.

24. The semiconductor integrated circuit of claim 21, wherein:

the master cell is a memory element having a variation output, the memory element including a variation detection circuit which outputs an original variation signal indicative of a variation occurred in the content of the master cell; and

the variation detection means includes the variation detection circuit and outputs the variation signal based on the original variation signal output by the variation detection circuit.

25. The semiconductor integrated circuit of claim 21, wherein:

the variation detection means includes a clock pulse generation request signal line for transmitting a request signal which requests the clock pulse generator to generate the clock pulse, the clock pulse generation request signal line changing the request signal to a first logic value when receiving the variation signal output by the variation detection means and changing the request signal to a second logic value when receiving a request update signal; and

the clock pulse generator is a clock pulse generator having an update output

which generates the clock pulse and the request update signal when the request signal is changed to the first logic value, the request update signal being supplied to the clock pulse generation request signal line.

26. A communication device comprising a semiconductor integrated circuit, wherein the semiconductor integrated circuit is the semiconductor integrated circuit of claim 21.

27. An information reproducing device comprising a semiconductor integrated circuit, wherein the semiconductor integrated circuit is the semiconductor integrated circuit of claim 21.

28. An image display device comprising a semiconductor integrated circuit, wherein the semiconductor integrated circuit is the semiconductor integrated circuit of claim 21.

29. An electronic device comprising a semiconductor integrated circuit, wherein the semiconductor integrated circuit is the semiconductor integrated circuit of claim 21.

30. An electronic controller comprising a semiconductor integrated circuit, wherein the semiconductor integrated circuit is the semiconductor integrated circuit of claim 21.

31. A movable apparatus comprising an electronic controller, wherein the electronic controller is the electronic controller of claim 30.